Claims

What is claimed is:

1. A method for data recovery, the method comprises the steps of:

a) receiving a stream of biphase encoded data, wherein the stream of biphase encoded data includes a plurality of frames;

b) determining whether a next transition of a frame of the plurality of frames occurs during a first, second, or third time window after a preceding transition of the frame;

c) synchronizing to a data rate of the stream of biphase encoded data based on the next transition and the preceding transition when the next transition occurred during the second time window; and

d) synchronizing to the data rate of the stream of biphase encoded data based on the preceding transition and a subsequent transition when the next transition occurred during the first or the third time window.

2. The method of claim 1, wherein steps (c) and (d) further comprise:

when the next transition occurred within the first or third time window, masking the next transition to a phase locked loop;

when the next transition occurred within the second time window, providing the next transition to the phase locked loop; and

synchronizing, by the phase locked loop, to a data rate of the stream of biphase encoded data based on the next transition and the preceding transition.

3. The method of claim 2 further comprises:

adjusting a dynamic divider based on the data rate and an output of the phase locked loop to produce a divider; and

producing a recovered data clock based on the output of the phased locked loop and the divider.

4. The method of claim 3, wherein the adjusting the dynamic divider further comprises:

determining a current count based on a number of clock cycles of the output of the phase locked loop that occur during a frame of the stream of biphase encoded data;

comparing the current count with a stored minimum count; and

decrementing the stored minimum count when the current count compares unfavorably to the stored minimum count.

5. The method of claim 4 further comprises:

incrementing the stored minimum count when the current count compares favorably to the stored minimum count.

6. The method of claim 4 further comprises

maintaining the stored minimum count when the current count matches the stored minimum count.

7. The method of claim 4 further comprises, prior to the phase locked loop being locked,:

determining whether the stored minimum count is less than a predetermined value;

decreasing rate of the phase locked loop when the stored minimum count is less than the predetermined value.

8. The method of claim 4 further comprises, prior to the phase locked loop being locked,:

determining whether the stored minimum count is greater than a predetermined value; and

increasing rate of the phase locked loop when the stored minimum count is greater than the predetermined value.

9. The method of claim 2, wherein step (b) further comprises:

counting a number of clock cycles of an output of the phase locked loop that occur between the preceding transition and the next transition;

determining that the next transition occurs during the first time window when the number of clock cycles is in a first range;

determining that the next transition occurs during the second time window when the number of clock cycles is in a second range; and

determining that the next transition occurs during the third time window when the number of clock cycles is in a third range.

10. A data recovery circuit comprises:

an edge detection module operably coupled to receive a stream of biphase encoded data, wherein the edge detection module detects edges of the stream of biphase encoded data and generates edge type information, and wherein the biphase encoded data includes a plurality of frames;

a reference module operably coupled to receive the stream of biphase encoded data and the edge type information and to produce, therefrom, a reference data rate signal;

a phase locked loop operably coupled to produce a system clock based on the reference data rate signal;

a lock detect module operably coupled to the phase locked loop, wherein the lock detect module generates a lock signal when the phase locked loop is in a steady state condition;

an operational control module operably coupled to receive the lock signal, the edges of the stream of biphase encoded data, and a recovered data clock and produces therefrom, a data clock control signal;

a data clock module operably coupled to receive the system clock and the data clock control signal and to produce, therefrom, the recovered data clock; and

a data format module operably coupled to receive the edges of the stream of biphase encoded data, the lock signal, and the recovered data clock and to produce, therefrom, an output data stream.

11. The data recovery circuit of claim 10, wherein the edge detection module further comprises:

a counter that counts a number of clock cycles of the system clock between consecutive edges of the stream of biphase encoded data; and

an edge interpreting module operably coupled to receive the number of clock cycles and to determine, therefrom, whether a current transition edge corresponds to at least one of: a clock edge, a data edge, and a preamble edge to produce the edge type information.

12. The data recovery circuit of claim 11, wherein the reference module is further operably coupled to generate an edge skip signal when the edge type information indicates that the current transition edge is one of the data edge and the preamble edge.

13. The data recovery circuit of claim 10, wherein the data clock module further comprises a dynamic divider, wherein the dynamic divider divides, based on the data clock control signal (e.g., is the minimum stored count), the system clock to produce a representation of the recaptured data clock.

14. The data recovery circuit of claim 13, wherein the data clock module further comprises a divider network to produce the recaptured data clock, a frame clock, and a block clock.

15. The data recovery circuit of claim 10, wherein the data clock control signal comprises at least one of: coarse clock adjust, fine clock adjust, and restart clock adjust.

16. The data recovery circuit of claim 10, wherein the operational control module further comprises:

a counter operably coupled to count the number of clock cycles of the system clock for a frame of the stream of biphase encoded data; and

a comparison module operably coupled to receive the number of clock cycles, wherein the comparison module compares the number of clock cycles with a minimum stored count and produces, therefrom, the data clock control signal.

17. The data recovery circuit of claim 10, wherein the lock detect module further comprises a comparator operably coupled to compare phase of the reference data rate signal with phase of a feedback signal against a PLL lock clock, wherein the PLL lock clock includes at least one of: a fine setting and a coarse setting.

18. A data recovery circuit comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to: (a) receive a stream of biphase encoded data, wherein the stream of biphase encoded data includes a plurality of frames; (b) determine whether a next transition of a frame of the plurality of frames occurs during a first, second, or third time window after a preceding transition of the frame; (c) synchronize to a data rate of the stream of biphase encoded data based on the next transition and the preceding transition when the next transition occurred during the second time window; and (d) synchronize to the data rate of the stream of biphase encoded data based on the preceding transition and a subsequent transition when the next transition occurred during the first or the third time window.

19. The data recovery circuit of claim 18 further comprises a phase locked loop and, wherein the memory further includes operational instructions that cause the processing module to:

mask the next transition to the phase locked loop when the next transition occurred within the first or third time window; and

provide the next transition to the phase locked loop when the next transition occurred within the second time window, such that the phase locked loop is synchronized to a data rate of the stream of biphase encoded data based on the next transition and the preceding transition.

20. The data recovery circuit of claim 19 further comprises a dynamic divider and, wherein the memory further includes operational instructions that cause the processing module to:

provide an adjustment signal to the dynamic divider based on the data rate and an output of the phase locked loop, such that the dynamic divider produces a divider; and

produce a recovered data clock based on the output of the phased locked loop and the divider.

21. The data recovery circuit of claim 20, wherein the memory further includes operational instructions that cause the processing module to produce the adjustment signal by:

determining a current count based on a number of clock cycles of the output of the phase locked loop that occur during a frame of the stream of biphase encoded data;

comparing the current count with a stored minimum count;

decrementing the stored minimum count when the current count compares unfavorably to the stored minimum count, wherein the adjustment signal is representative of the stored minimum count;

incrementing the stored minimum count when the current count compares favorably to the stored minimum count; and

maintaining the stored minimum count when the current count matches the stored minimum count.

22. The data recovery circuit of claim 20, wherein the memory further includes operational instructions that cause the processing module to, prior to the phase locked loop being locked:

determine whether the stored minimum count is less than a predetermined value;

provide a decrease rate signal to the phase locked loop when the stored minimum count is less than the predetermined value.

23. The data recovery circuit of claim 20, wherein the memory further includes operational instructions that cause the processing module to, prior to the phase locked loop being locked:

determine whether the stored minimum count is greater than a predetermined value; and

provide an increase rate signal to the phase locked loop when the stored minimum count is greater than the predetermined value.